Amendments to the Specification

Please replace paragraph [0009] with the following amended paragraph:

In the example of FIG. 1, the illustrated interrupt dispatch system 100 includes a plurality of processors 110, generally shown as Processors #1 through N 120, 130, and 140, respectively. Each of the plurality of processors 110 includes a local programmable interrupt controller (LPIC), generally shown as 122, 132, and 142. Each of the LPICs 122, 132, and 142 includes an inter-processor interrupt register (IPIR), generally shown as ~~124~~ 126, ~~134~~ 136, and ~~144~~ 146, and an interrupt control register (ICR), generally shown as ~~126~~ 124, ~~136~~ 134, and ~~146~~ 144. The LPICs 122, 132, and 142 handle pending interrupts, masking, prioritization, and vector generation as persons of ordinary skill in the art will readily recognize. In particular, the LPICs 122, 132, and 142 (e.g., via the ICRs ~~126~~ 124, ~~136~~ 134, and ~~146~~ 144, respectively) receive and process inter-processor interrupt (IPI) messages for the cores of the plurality of processors 110 to execute. The LPICs 122, 132, and 142 (e.g., via the IPIRs ~~124~~ 126, ~~134~~ 136, and ~~144~~ 146, respectively) also generate IPI messages to enable the plurality of processors 110 to communicate with each other.

Please replace paragraph [0019] with the following amended paragraph:

Upon calculating the IWAs 260 by the WAG 250, the TPS 270 compares the IWAs 260 of the plurality of processors 110 to select one of the plurality of processors 110 as the target processor for receiving/servicing a next interrupt. For example, the TPS 270 may identify the processor associated with the highest IWA as the target processor. In that case, the MPIC 160 dispatches the interrupt to the target processor to execute by generating an IPI message to the target processor identifier (TPID) ~~262~~ 272 of the target processor.